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(71)**Name of Applicant :**
1)Chitkara University
Address of Applicant :Chitkara University, Chandigarh - Patiala National Highway, Village Jhansla, Rajpura, Punjab - 140401, India. Patiala ---------- ----------
2)Chitkara Innovation Incubator Foundation
Name of Applicant : NA
Address of Applicant : NA
(72)**Name of Inventor :**
1)BATT, Suhaib Ahmed
Address of Applicant :Chitkara University Institute of Engineering and Technology, Chitkara University, Chandigarh - Patiala National Highway, Village Jhansla, Rajpura, Punjab - 140401, India. Patiala ---------- ----------

(57) Abstract :
The present disclosure relates to a shift register system (200). The system comprises one or more configurable circuits configured with the shift register system for performing operations based on a data configuration. The system also includes one or more flip flops configured to shift data received through the data configuration based on a clock signal. The system provides a 3-input majority voter (3MV) gate configured with one or more flip flops for receiving an input signal and latching a signal associated with an input signal to the port of one or more flip flops when the clock signal of a predetermined logic is detected. The system provides an output signal associated with the output port of the one or more flip flops when the clock signal of the predetermined logic is detected.

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