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(57) Abstract :
The present invention discloses a power-efficient CMOS transistor circuit (100) configured as a 4:2 compressor is disclosed. This circuit (100) significantly reduces power consumption and optimizes transistor count, making power efficient approximate 4:2 compressor ideal for image processing applications. The design maintains adequate accuracy metrics, making it a valuable asset in the field of digital signal processing. The compressor excludes the use of an EXOR gate, a common feature in traditional designs, opting instead for a more efficient and compact approach. The core of this compressor is its unique CMOS circuit configuration, which significantly reduces the number of transistors required.

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