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(57) Abstract :
The present disclosure relates to a Carbon Nano-Tube Field Effect Transistor (CNTFET) and more specifically, relates to a design and functionality of the CNTFET based memory bit-cell (100). The memory bit-cell (100) features two transistors with their inputs connected to each other's outputs, establishing a latch for data storage. The transistors (M1) – (M4), create a back-to-back configuration, ensuring the retention of current data. To address access transistor sizing conflicts, the widely accepted read decoupled technique is employed, utilizing transistors (M5) and (M6). Furthermore, the VGND control signal is utilized to minimize sub-threshold leakage current. The one-sided inverter weakening technique is applied, with transistor (M7) playing a pivotal role in weakening the left inverter during write 1 operation, facilitating the transition of node Q from 0 to 1. It is imperative for the write line (WL) signal to remain high during write operations, necessitating the activation of transistor (M8).

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