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(57) Abstract :  
 The present disclosure provides a data center security system (100) include a multitude of server systems on a chip (SOCs), each housing an integrated processor (104) and a memory (106) on a single chip. The memory (106) holds executable instructions that prompt the processor to perform tasks such as analyzing data traffic, system behavior, and security events at the chip level. In response to security breaches or suspicious activities, the processor triggers security responses within the server SOCs, sending alert signals to an entity (114). Moreover, the processor (104) generates security audit logs and reports based on activities within the associated server SOCs. A central controller (108) communicatively connected to the server SOCs and configured to effectively manage and coordinate security operations of each processor across the collective server SOCs.

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