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(57) Abstract :
A method for generating clock glitches 202 includes a digital circuit, a data processing unit to perform operations of identifying edge-triggered devices in an original register-transfer level file of the digital circuit design, generating a clock glitch 202 with one or more algorithms, defining clock glitch 202 parameters in terms of the time of the glitch 204 and width of glitch 206, and controlling them by modifying given codes, flip-flops as edge-triggered devices, and a receiving register receiving a clock domain crossing signal on at least one input. The digital circuit further uses an algorithm to automatically detect incorrect output of said circuit design related to an undesirable effect of setup and hold time violations in flip-flops and the algorithm is automatically generated.

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