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(57) Abstract :

The present disclosure relates to a method of fabricating a graphene tunnel field effect transistor. The method growing a first layer on a silicon carbide that acts as a buffer layer (comprises energy band gap of 0 eV), and the second graphene layer comprises energy band gap of -0.26 eV. The p-source, δ -channel, and δ -drain region in the second graphene layer are formed by using a source polarity gate metal, a control gate metal electrode, and a drain polarity gate metal, respectively. Insulating the source polarity gate metal and control gate metal electrode from each other and the second graphene layer using a high- ϵ dielectric, wherein a control gate metal electrode and a drain polarity gate metal from each other and the second graphene layer using a carbon allotrope (Diamond-like Carbon).

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