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(57) Abstract :
In the present invention, the inventors have integrated the expertise of electronics researcher and Arithmetic Logic Unit to develop low cost, low power and secure hardware based Vedic Multiplier design for applications like Digital Signal processing. The Vedic multiplier is designed on the basis of Urdhva Tiryagbhyam sutra of Vedic mathematics. In order to make Vedic multiplier time efficient, speedy and having lesser area, are implemented in Arithmetic and Logical Units replacing the traditional multipliers and squares based on array and Booth multiplication. In order to make them energy efficient, techniques like voltage scaling, thermal scaling and process variation have been used for LVTTL, PCI, GTL and HSUL IO standards for energy efficient Vedic multiplier.

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