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(57) Abstract :
In the present invention, the inventors have integrated the expertise of electronics researcher and natural language processing researcher in order to develop faster, low cost, low power and secure hardware based Unicode reader design for 22 languages of eighth schedule of constitution of India. In order to make the processing faster, core electronics techniques like clock dedicated route, directed routing, area group compression, mapping, finite state machine, controlling skew, jitter and delay for high performance Unicode reader design are used. In order to make them energy efficient, core electronics techniques like clock gating, capacitance scaling, voltage scaling, thermal scaling, IO standard, impedance matching, mobile DDR I/O standard, HSTL I/O Standard, DCI, SSTL and LVCMOS for energy efficient Unicode reader design are being used.

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