

(12) PATENT APPLICATION PUBLICATION

(21) Application No.202011013726 A

(19) INDIA

(22) Date of filing of Application :28/03/2020

(43) Publication Date : 01/10/2021

(54) Title of the invention : CIRCUIT FOR NOISE MITIGATION

(51) International classification	:G11C0027020000, H03K0017160000, H01L0027120000, H03F0001260000, H03K0019003000	(71) <b>Name of Applicant :</b> <b>1)Chitkara Innovation Incubator Foundation</b> Address of Applicant :SCO: 160-161, Sector - 9c, Madhya Marg, Chandigarh- 160009, India. Chandigarh India
(31) Priority Document No	:NA	(72) <b>Name of Inventor :</b>
(32) Priority Date	:NA	<b>1)SHARMA, Kulbhushan</b>
(33) Name of priority country	:NA	<b>2)SHARMA, Rajnish</b>
(86) International Application No	:NA	
Filing Date	:NA	
(87) International Publication No	: NA	
(61) Patent of Addition to Application Number	:NA	
Filing Date	:NA	
(62) Divisional to Application Number	:NA	
Filing Date	:NA	

(57) Abstract :

The present disclosure provides a circuit 100 for noise mitigation. The circuit 100 comprises an input terminal 110, through which an input signal is applied, a noise control unit 120, to control the level of noise in the input signal, an output terminal 130, which provides a filtered signal. The noise control unit 120 includes a transistor 122, a capacitor 124, and a resistor 126, such that the capacitor 124 is configured between a body terminal B and a gate terminal G of the transistor 122. The input signal is applied to a gate terminal G and a body terminal B, through the capacitor 124, of the transistor 122, where the configured combination of the transistor 122 and the capacitor 124 enables the circuit 100 to control the level of noise in the input signal, and, further, the filtered signal can be collected from the output terminal 130.

No. of Pages : 17 No. of Claims : 10