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(57) Abstract :

Inventors have developed 32 X 64 bit QCA based SRAM using eleven input majority gates and successfully designed addressing circuitry i.e. 32:1 multiplexer and 5 X 32 decoders for the memory design. This newly developed 32 X 64 bit SRAM can be designed from lesser number of QCA cells thereby reducing the circuit complexity and lesser area is thus occupied as compared to the existing technology.

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